REMARKS

Claims 1-4, 6, 7, and 9-14 are pending. Claims 1, 4 and 9 have been amended. Reconsideration and allowance of the present application based on the following remarks are respectfully requested.

Entry of this Amendment is respectfully requested since no new issues are raised by entry and it places the Application in condition for allowance, or at least in better form for appeal.

In the Specification

The specification was objected to because a typographical error was present in the May 20, 2005 amendment. Applicant has resubmitted the amendment herewith to correct the error. Accordingly, Applicant respectfully requests reconsideration and withdrawal of this objection.

Claim Objections

Claim 4 was objected to for containing a typographical error. Applicants have amended claim 4 to correct this error. Accordingly, Applicant respectfully submits that this objection is moot.

Claim Rejections Under 35 U.S.C. § 103

Claims 1-4, 6, and 7 were rejected under 35 U.S.C. § 103(a) over Yanagawa (U.S. Patent No. 5,843,848) in view of Brown et al. (U.S. Patent No. 6,541,320) and further in view of Jang et al. (U.S. Patent No. 5,518,959); claims 9-14 were rejected under 35 U.S.C. § 103(a) over Yanagawa in view of Jang; and claims 1-4 and 6-7 and 9-14 were rejected under 35 U.S.C. § 103(a) over Narita et al.(U.S. Patent No. 6,383,942) in view of Jang. Applicant respectfully traverses these rejections.

Amended claim 1 recites a method of forming a metal line layer in a semiconductor device that includes depositing a diffusion barrier layer, a metal layer and an anti reflection layer on a semiconductor substrate, depositing an insulating film on the anti reflection layer, depositing and patterning a photosensitive material on the insulating film, etching portions of the insulating film, the anti reflection layer and the metal layer using activated plasma and the photosensitive material as a mask, whereby a portions of side walls of the metal layer are over-etched by plasma ions, removing the photosensitive material, forming a side wall oxide film on

the over-etched side walls of the metal layer by reacting the metal layer with ozone and etching portions of the diffusion barrier layer using the insulating film and the side wall oxide film as an etch mask.

The Office Action admits that Yanagawa does not teach a side wall oxide film on the over-etched side walls of the metal layer by reacting the metal layer with ozone and portions of the diffusion barrier layer using the insulating film as an etch mask. However, the Office Action asserts that it in view of Jang, it would have been obvious to one of ordinary skill in the art to have formed a side wall oxide film on the over etched side walls of the metal layer by reacting the metal layer with ozone and to have had the sidewall oxide film be Al_2O_3 in the method of Yanagawa. Applicants respectfully disagree.

Jang is concerned with an improved method for forming a gap filling and planarizing silicon oxide insulator spacer layer within patterned metal layers. Therefore, Jang provides a silicon oxide insulator spacer layer 5a, 5b, 5c which is formed selectively upon the exposed surfaces of a silicon oxide insulator substrate layer 1 and upon sidewalls of three layer patterned metal stacks 2a, 2b, 3a, 3b, 4a, 4b (Col. 4 line 15-24, fig. 1) by controlling a deposition time not exceeding an incubation time for forming the silicon oxide insulator spacer layer 5a, 5b, 5c upon the top barrier metal layer 4a, 4b formed from titanium nitride (line19-23 at Abstract). Therefore, the side wall oxide film 230 is formed in order to mitigate an etch damage of the side wall of the metal layer in the invention of claim 1, while the silicon oxide insulator spacer layer5a, 5b, 5c is formed in order to fill gap within patterned metal stacks and in order to prohibit diffusion of the metal stacks in Jang's invention. Also, the side wall oxide film 230 is formed on the over-etched side walls of the metal later 210b, not on the anti reflector layer, diffusion barrier layer and substrate, in the invention of claim 1, while the silicon oxide insulator spacer layer 5a, 5b, 5c is formed not only on the edges of patterned conductor metal layer 3a, 3b but also on the silicon oxide insulator substrate layer 1, edges of patterned lower barrier metal layer 2a, 2b and edges of patterned upper barrier metal layer 4a, 4b in Jang's invention. Further, portions of the diffusion barrier layer 210a are etched using the insulating film and the side wall oxide film 210b as an etch mask in the invention of claim 1, while the silicon oxide insulator spacer layer 5a, 5b, 5c is not used for etch mask in Jang's invention.

Additionally, Brown teaches that a patterned mask 56 protects underlying layers from subsequent etching processes and is used in defining the gate region (Col. 4 line 32-34).

However, claim 1 of the present invention teaches that the insulating film 212 is used for etching portions of the diffusion barrier layer not defining the gate region. Also, claim 1 recites that insulating film 212 and the side wall film 230 are used as etch mask. Accordingly, Brown does not teach or even suggest that etching portions of the diffusion barrier layer using the insulating film and the side wall oxide film as an etch mask.

Amended claim 9 recite a method of forming a metal line layer in a semiconductor device, comprising depositing a first, second and third conductive layers on a semiconductor substrate, depositing an insulating film on the third conductive layer, dry etching portions of the insulating film, the third and the second conductive layers using activated plasma, whereby a portions of side walls of the second conductive layer are over-etched by plasma ions, forming a side wall oxide film on the side walls of the over-etched second conductive layer by reacting the second conductive layer with ozone and etching portions of the first conductive layer using the insulating film and the side wall oxide film as an etch mask.

As discussed above with respect to claim 1, Yanagawa and Jang do not teach or even suggest that forming a side wall oxide film on the side walls of the over-etched second conductive layer by reacting the second conductive layer with ozone and etching portions of the first conductive layer using the insulating film and the side wall oxide film as an etch mask.

Claim 9 is believed allowable for at least the same reasons presented above with respect to claim 1 since claim 9 recites features that are similar to the features of claim 1 and because Narita does not remedy those deficiencies. Accordingly, no combination of Yanagawa, Brown, Jang, and Narita teach or suggest the subject matter of claims 1 and 9.

Claim 2-4, 6, 7, and 10-14 are believed allowable for at least the reasons presented above with respect to claims 1 and 9 by virtue of their dependence upon claims 1 and 9. Accordingly, Applicant respectfully requests reconsideration and withdrawal of these rejections.

Conclusion

Therefore, all objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Should any issues remain unresolved, the Examiner is encouraged to contact the undersigned attorney for Applicants at the telephone number indicated below in order to expeditiously resolve any remaining issues.

Respectfully submitted,

MAYER BROWN ROWE & MAW LLP

By: _____ Reg No. 51,873
for Yoon S. Ham
Registration No. 45,307
Direct No. (202) 263-3280

YSH/VVK

Intellectual Property Group
1909 K Street, N.W.
Washington, D.C. 20006-1101
(202) 263-3000 Telephone
(202) 263-3300 Facsimile

Date: March 21, 2006